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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,648	12/31/2001	Howard S. David	42390.P12981	9206

8791 7590 03/24/2004

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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2186	6

DATE MAILED: 03/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,648	DAVID, HOWARD S.	
	Examiner	Art Unit	
	Zhuo H Li	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office action is in response to the amendment filed on December 31, 2001 (Paper No.).

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claim 1 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/039,580 field on December 31, 2001. Although the conflicting claims are not identical, they are not patentably distinct from each other because all the claimed features of the present Application 10/039,648 are transparently found in co-pending Application 10/039,580.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-5 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding claim 1, the newly amended limitation "the command sequencer and serializer unit to reduce a first plurality of address and command signals down to a more narrow set of signal lines coupled to the memory module, the more narrow set of signal lines forming a point-to-point interconnect between the command sequencer and serializer unit and the memory module" is neither clearly disclosed in the drawing nor described in the specification. If

applicant believe it does disclosed in at the time the application was filed, please point it out to the examiner with the detail page and line numbers in the response.

Regarding claims 2-5 are also rejected because of depending on claim 1, containing the same deficiency.

The following art rejections are applied from what is best understood of the claim(s) in view of the 112 First paragraph problems listed above.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stracovsky et al. (US PAT. 6,216,178 hereinafter Stracovsky) in view of Saulsbury et al. (US PAT. 6,128,702 hereinafter Saulsbury.

Regarding claim 1, Stracovsky discloses an apparatus, i.e., system (100, figure 1B) comprising an array of tag address storage locations, i.e., resource tags (114, figure 1B), and a command sequencer and serializer unit, i.e., command sequencer (116, figure 1B), the command sequencer control a memory module, i.e., shared memory (108, figure 1B), the command sequencer to reduce a first plurality of address and command signals down to a more narrow set of signal lines coupled to the memory module, the more narrow set of signal lines forming a

point-to-point interconnect between the command sequencer and serializer unit and the memory module, i.e., the command sequencer is one of the component located in the universal controller as define in figure 1B, wherein the universal controller is able to received the requested commands and data signals from a plurality of processors (102, figure 1D) via the system bus (106, figure 1D), and further transfer the requested to the shared memory via the sequenced universal command (220, figure 1D), in addition, the universal controller having a system interface (110 figure 1D) arranges to covert the received system command and system address from the multiple processors, and further compares with a look up table in communicate with the resource tags, and comparator (122, figure 1D), further transfer the higher priority requested to the respective memory module via the unidirectional command bus (912, figure 9A) and bi-directional data bus (914, figure 9A) in order to avoid data collisions or other type conflicts (col. 5 line 49 through col. 8 line 64 and col. 9 lines 2-15). Stracovsky differs from the claimed invention in not specifically teaches a data cache located on a memory module. However, Saulsbury discloses a system (100, figure 1) comprising a memory controller, i.e. CPU (102) and a system memory (103, figure 1) wherein the system memory comprising a plurality of memory block (104, figure), and each memory block comprising data cache bank (122, figure 1) and main memory bank (118, figure 1). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory module of Stracovsky in having a data cache located on a memory module, as per teaching by the system of Saulsbury, because it reduces the miss rate and increase the access speed of in the memory operation.

Regarding claim 2, Saulsbury discloses the apparatus further comprising a plurality of arrays of tag address storage locations, each of the plurality of arrays of tag address storage

locations corresponding to one of a plurality of memory modules, i.e., each tag identifies the row in the corresponding memory bank 118, (col. 7 lines 41-61).

Regarding claims 3-4, Saulsbury discloses each of the plurality of arrays of tag address storage locations organized into a plurality of ways and 4 ways (col. 3 lines 54-63).

Regarding claims 5, Stracovsky discloses the more narrow set of signal lines including a plurality of command and address lines with the highly priority accessing value (col. 11 line 57 through col. 12 line 19).

Regarding claim 7, Stracovsky discloses a memory module, i.e., system shared memory (108) comprising a plurality of memory bank, i.e., device type 1 – device type N (figure 1C), the memory banks are controlled by commands delivered by a memory controller, i.e., universal controller (104, figure 1B) over a memory bus (220, figure 1B), the memory controller component including an array of tag address storage locations, i.e., resource tags (114, figure 1B), the memory controller component not located on the memory module, i.e., memory controller arranged to act as a liaison between a processor and shared memory (figure 1 B and col. 6 line 21 through col. 7 line 55). Stracovsky differs from the claimed invention in not specifically teaches a data cache coupled to the memory device wherein the data cache is located on the memory module. However, Saulsbury discloses a system (100, figure 1) comprising a memory controller, i.e. CPU (102) and a system memory (103, figure 1) wherein the system memory comprising a plurality of memory block (104, figure), and each memory block comprising data cache bank (122, figure 1) and main memory bank (118, figure 1). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory module of Stracovsky in having a data cache located on a memory

module, as per teaching by the system of Saulsbury, because it reduces the miss rate and increase the access speed of in the memory operation.

Regarding claim 8, Saulsbury discloses the apparatus further comprising a command decoder and the serializer, i.e., decoder (124, figure 2), to receive command and address information from the memory controller component, i.e., data cache bank control state machine (152) send out the W/R control commands and address (A20-A9) information via the bus 12 to the decoder (124), the command decoder and de-serializer unit providing control for the data cache, memory device (123, figure 2) provides requested address to the data cache storage (144).

Regarding claim 9, the limitations of the claim are rejected as the same reasons set forth in claims 3-4.

Regarding claim 10, Stracovsky discloses a system (100, figure 1B) comprising a processor (102, figure 1B), a memory controller, i.e., universal controller (104, figure 1B) coupled to the processor via the system bus (106, figure 1B), the memory controller including an array of tag address storage locations, i.e., resource tags (114, figure 1B), and a memory module, shared memory (108, figure 1B) separate from and coupled to the memory controller via a memory bus (220, figure 1B). Stracovsky differs from the claimed invention in not specifically teaches the memory module including a memory device, and a data cache coupled to the memory device, the data cache controlled by commands delivered by the memory controller. However, Saulsbury teaches in the computer system (100, figure 1) comprising a memory controller, i.e. CPU (102) and a system memory (103, figure 1) wherein the system memory comprising a plurality of memory block (104, figure), and each memory block comprising data cache bank (122, figure 1) and main memory bank (118, figure 1), in addition, Saulsbury teaches the

memory controller is able to accessing the data from the data cache memory via the primary data cache bank logic (150, figure 2). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory device of Stracovsky in having a memory device, and a data cache coupled to the memory device, the data cache controlled by commands delivered by the memory controller, as per teaching by the system of Saulsbury, because it reduces the miss rate and increase the access speed of in the memory operation.

Regarding claim 11, Stracovsky discloses the memory bus including a point-to-point interconnect to coupled the memory controller to the memory module via the bus (912 and 914, figure 9A) and (col. 11 line 55 through col. 12 line 19).

Regarding claim 12, Stracovsky discloses the memory controller (104, figure 1B) further including a plurality of arrays of tag address storage locations, i.e., resource tags (114, figure 1B) and (col. 7 line 25 through col. 8 line 2).

Regarding claim 13, Saulsbury discloses the system further comprising a plurality of memory modules, i.e., memory block (104, figure 1), each of the plurality memory modules including at least one of a plurality of memory devices, i.e., main memory bank (118, figure 1) and one of a plurality of data caches, i.e., primary data cache (122, figure 1), each of the data caches controlled by commands delivered by the memory controller, i.e., CPU (102, figure 1).

Regarding claim 14, Saulsbury discloses the plurality of arrays of tag address storage locations and the plurality of data caches organized into four ways (col. 3 lines 54-63).

Regarding claim 15, Stracovsky discloses a method comprising receiving a read request at a memory controller (104, figure 1B) from processor (102, figure 1B) via the system bus (106,

figure 1B), performing a tag look-up with the memory controller to determine whether there is a hit for the read request in the memory (col. 7 line 25 through col. 8 line 2), fetching the data from the memory if the tag look-up indicates a hit, the memory module separate from the memory controller and coupled to the memory controller via a memory bus (220, figure 1B). Stracovsky differs from the claimed invention in not specifically teaches the memory module including a data cache, the data cache controlled by commands delivered by the memory controller. However, Saulsbury teaches in the computer system (100, figure 1) comprising a memory controller, i.e. CPU (102) and a system memory (103, figure 1) wherein the system memory comprising a plurality of memory block (104, figure), and each memory block comprising data cache bank (122, figure 1) and main memory bank (118, figure 1), in addition, Saulsbury teaches the memory controller is able to accessing the data from the data cache memory via the primary data cache bank logic (150, figure 2). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory device of Stracovsky in having a data cache coupled to the memory device, the data cache controlled by commands delivered by the memory controller, as per teaching by the system of Saulsbury, because it reduces the miss rate and increase the access speed of in the memory operation.

Regarding claim 16, Saulsbury discloses the method further comprising loading a line of data from a memory device located on the memory module to the data cache if the tag look-up indicates a cache miss via the cache line bus (4096), and delivering the line of data to the memory controller (col. 11 line 59 through col. 12 line 2).

Response to Arguments

8. Applicant's arguments with respect to claims 1-5 and 7-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H Li whose telephone number is 703-305-3846. The examiner can normally be reached on Tue-Fri 9:00 a.m. to 6:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 703-305-3821. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Zhuo H. Li

March 19, 2004

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100